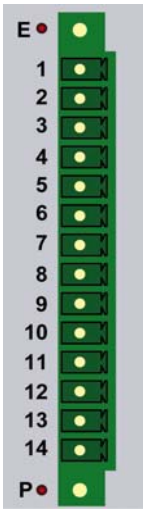
# analog input fft 3403

- **16 bit analog input**
- **± 10V**
- **4 channels, simultaneous sampling**
- **differential input**
- **galvanicaly isolated**

I/O

## Pinout

| | | |
|---|---|---|
| **LED:** | 0; (8) | Ch0/FIFO0: positive input voltage |
| | 1; (9) | Ch1/: positive input voltage |
| | 2; (10) | Ch2: positive input voltage |
| | 3; (11) | Ch3: positive input voltage |
| | 4; (12) | Ch0: negative input voltage |
| | 5; (13) | Ch1: negative input voltage |
| | 6; (14) | Ch2: negative input voltage |
| | 7; (15) | Ch3: negative input voltage |
| | E: | failure, red |
| | P: | power supply, red |




| Pin | Signal |
|---|---|
| 1 | Ch0+ |
| 2 | Ch0- |
| 3 | AGND |
| 4 | Ch1+ |
| 5 | Ch1- |
| 6 | AGND |
| 7 | Ch2+ |
| 8 | Ch2- |
| 9 | AGND |
| 10 | Ch3+ |
| 11 | Ch3- |
| 12 | AGND |
| 13 | Power +24V= |
| 14 | Power 0V |

## Attributes

**Dataformat:**
Standard integer (16-Bit) format :
+32767= +10V
0 = 0V
-32768 = -10V

**Applications:**
16 bit analog input, voltage sensing, continious sampling of one selectable channel results readable from fifo register available prints :

- @P3403L: 4 channels, 16 bit analog input, fifo, ±10V
- @P3403R: 4 channels, 16 bit analog input, fifo, ±10V

analog

input

**Related Applications:**
2 channels, voltage sensing:

- @P3400: 4 channels, 16 bit analog input, ±10V

2/4 channels, current sensing:

- @P3210: 2 channels, 16 bit analog input, ±20mA
- @P3410: 4 channels, 16 bit analog input, ±20mA

## Electrical Data

Power supply external ..... 24V= ± 20%
Operating Current ..... 40mA at 24V=, typical
Operating current @ctiveBus .....
Input protection ..... 30V overvoltage, surge
Differential input voltage ..... 60V, maximum
Input resistance ..... 1MΩ
Input capacity ..... 160nF
Maximum sampling frequency ..... 20kHz
Input frequency .....
Resolution / Accuracy ..... 16 bit / 13 bit
No. of converters ..... 4, simultaneous sampling, no multiplexers

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## System Information

System ID .....0x0288
System address space .....96 bit in, 96 bit out

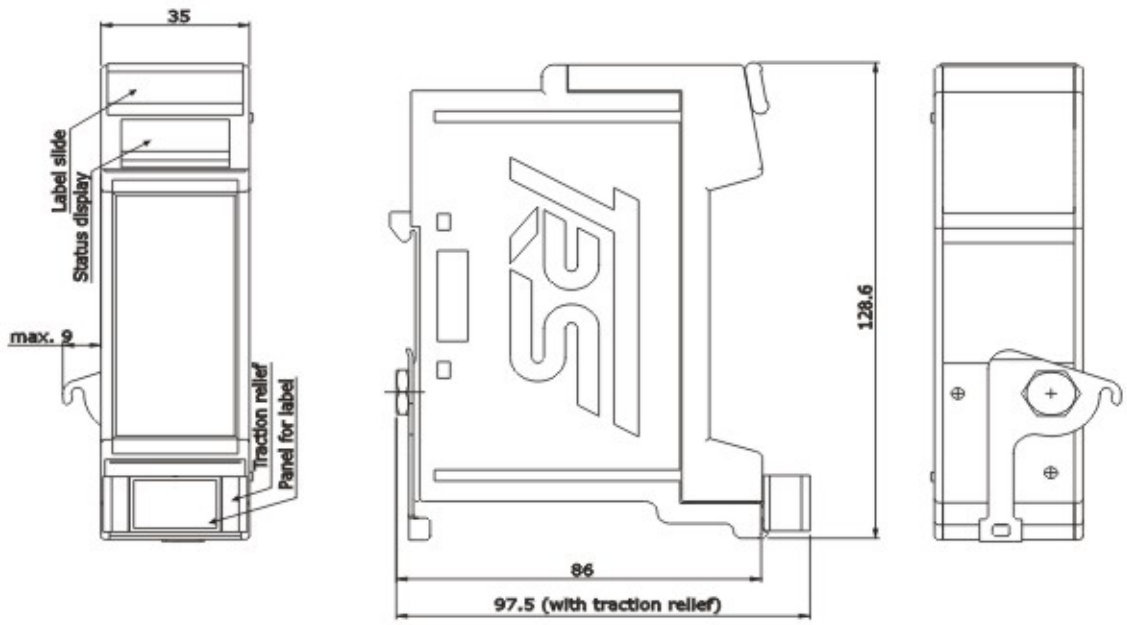
## Environmental Conditions

Electromagnetic compatibility (EMC) .....EN 61000-4-2 (IEC-801-2) / EN 61000-4-4 (IEC-801-4)
Operating temperature [°C] .....0 .. +55
Storage temperature [°C] .....-20 .. +70
Humidity (rel) .....98 % (non condensing)
Protection class*.....IP 20 (DIN 40 050)
*The protection class is valid only with housing and connector installed

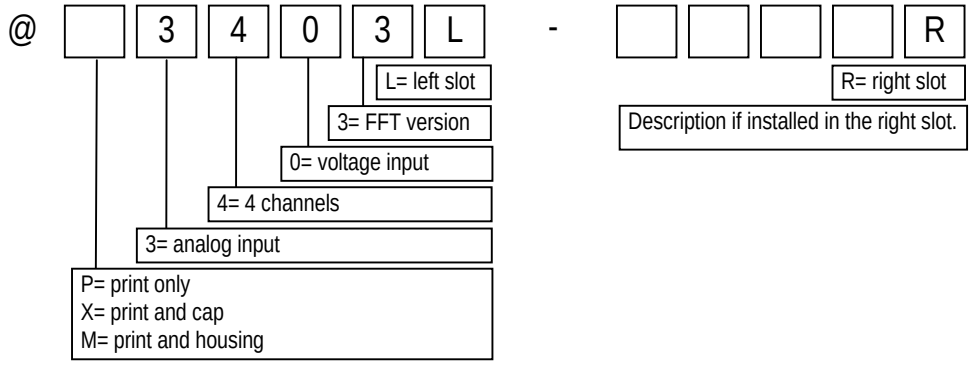
## Mechanical Data PCB

Weight .....approx. 0.05 kg including connector
Dimension .....105mm x 80mm x 12mm

## Drawing **(effective if mounted in @M housing)**




## Ordering Key

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**notes:**

Read Status Bits (this bits are mirrored from data bits 80-95):

Table 1: Status bits

| Bit | Name | Description |
|---|---|---|
| 0 | Version Bit 0 | Version info of FPGA |
| 1 | Version Bit 1 | |
| 2 | Version Bit 2 | |
| 3 | Version Bit 3 | |
| 4 | WR_DATA_INFO | |
| 5 | EN_FIFO | If EN_FIFO=1:<br>Data Register DATA_A to DATA_D contains sampling value of selected channel in hierarchial order DATA_A t=0, DATA_B t=-1, DATA_C t=-2, DATA_D t=-3 |
| 6 | CH_SOURCE0 | Select source for fifo register: 00 channel A, 01 channel B, 10 channel C, 11 channel D |
| 7 | CH_SOURCE1 | |
| 8 | S_CLOCK0 | Sampling clock of ADC |
| 9 | S_CLOCK1 | |
| 10 | S_CLOCK2 | |
| 11 | OVF | Overflow fifo |

**Write Parameter Bits:**

Table 2: Parameter bits

| Bit | Name | Description |
|---|---|---|
| 0 | Parameter enable | must be set high to change any function |
| 1 | not defined | |
| 2 | not defined | |
| 3 | not defined | |

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**notes:**

**Read DATA (Default Mode):**

Table 3: Default data read

| Bit | Name | Description |
|---|---|---|
| 15-0 | DATA_A | analog value of channel A |
| 31-16 | DATA_B | analog value of channel B |
| 47-32 | DATA_C | analog value of channel C |
| 63-48 | DATA_D | analog value of channel D |
| 79-64 | FIFO_STAGE4 | stage four of the FIFO |
| 95-80 | CONTROL | control bits and sample counter, bit 95-88 is mirrored on status-bit 11-4 |
| | | |

**Write Data:**

Table 4: Data write

| Bit | Name | Description |
|---|---|---|
| 15-0 | res | only readable |
| 31-16 | res | only readable |
| 47-32 | res | only readable |
| 63-48 | res | only readable |
| 79-64 | res | only readable |
| 95-80 | CONTROL | control word see below |

Read DATA (en_fifo=1):

Table 5: Data read (mode fifo)

| Bit | Name | Description |
|---|---|---|
| 15-0 | FIFO_STAGE0 | analog value of selected channel t = 0 |
| 31-16 | FIFO_STAGE1 | analog value of selected channel t = -1 |
| 47-32 | FIFO_STAGE2 | analog value of selected channel t = -2 |
| 63-48 | FIFO_STAGE3 | analog value of selected channel t = -3 |
| 79-64 | FIFO_STAGE4 | analog value of selected channel t = -4 |
| 95-80 | CONTROL | control word see below |

Table 6: Control word

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | cnt7 | cnt6 | cnt5 | cnt4 | cnt3 | cnt2 | cnt1 | cnt0 |

Table 7: Control word

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| | ovf | clk2 | clk1 | clk0 | ch1 | ch0 | en_fifo | wr_en |

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**notes:**

**cnt7-cnt0:** .....8-bit counter, will be incremented on each sampling

**wr_en:**.....Write enable, must set 1 for any changes of control word bit 15-9

**en_fifo:** .....Change modul to fifo mode, bit 64-0 contains values of selected channel in hierarchical order

**ch1-ch0:**

| Ch1 | Ch 0 | Selected channel |
|---|---|---|
| 0 | 0 | A |
| 0 | 1 | B |
| 1 | 0 | C |
| 1 | 1 | D |

**clk2-clk0:**

| Clk2 | Clk1 | Clk0 | Sample frequency |
|---|---|---|---|
| 0 | 0 | 0 | 20 kHz |
| 0 | 0 | 1 | 10 kHz |
| 0 | 1 | 0 | 5 kHz |
| 0 | 1 | 1 | 2.5 kHz |
| 1 | 0 | 0 | 1.25 kHz |
| 1 | 0 | 1 | triggered by systembus transfer |
| 1 | 1 | 0 | reserved |
| 1 | 1 | 1 | reserved |

**ovf:**

| | |
|---|---|
| **Read** | Overflow fifo, systembus transfer period is longer than time of five **adc**-samples -> some samples are lost<br>You should set this bit high until you start buffering of the **adc** samples |
| **Write** | Write ovf = 1 reset over flow fifo counter |
| | Write ovf = 0 enable count mode overflow fifo counter |